CLAIMS

What is claimed is:

1. A core for providing communications between a transmission media and a processor in a parallel-serial architecture, said core comprising:

serial lanes connecting said processor to said transmission media; and

at least one selector connected to said serial lanes, whereby said selector selectively engages said serial lanes to alter a speed of data passing through said core.

2. The core in claim 1, further comprising a data controller for controlling an operation of said selector.

3. The core in claim 1, wherein said serial lanes include buffers for performing additional speed alteration of said data.

4. The core in claim 3, wherein said buffers comprise elastic first-in, first-out (FIFO) buffers.

5. The core in claim 1, wherein said selector comprises a multiplexor.

6. The core in claim 1, wherein additional speed adjustment is attained by said selector engaging additional lanes.

7. The core in claim 1, wherein said transmission media operates at a different data speed than said processor.

8. A parallel-serial communication system comprising:

at least one processor;

at least one transmission media connecting said at least one processor; and

a core between each processor and said transmission media, said core providing communications between said transmission media and said, and said core comprising:

serial lanes connecting said processor to said transmission media; and

at least one selector connected to said serial lanes, whereby said selector selectively engages said serial lanes to alter a speed of data passing through said core.

9. The parallel-serial communication system in claim 8, further comprising a data controller for controlling an operation of said selector.

10. The parallel-serial communication system in claim 8, wherein said serial lanes include buffers for performing additional speed alteration of said data.

11. The parallel-serial communication system in claim 10, wherein said buffers comprise elastic first-in, first-out (FIFO) buffers.

12. The parallel-serial communication system in claim 8, wherein said selector comprises a multiplexor.

13. The parallel-serial communication system in claim 8, wherein additional speed adjustment is attained by said selector engaging additional lanes.

14. The parallel-serial communication system in claim 8, wherein said transmission media operates at a different data speed than said processor.

15. A core for providing communications between a transmission media and a processor in a byte-stripped parallel-serial InfiniBand architecture, said core comprising:

serial lanes connecting said processor to said transmission media; and

at least one selector connected to said serial lanes, whereby said selector selectively engages said serial lanes to alter a speed of data passing through said core.

16. The core in claim 15, further comprising a data controller for controlling an operation of said selector.

17. The core in claim 15, wherein said serial lanes include buffers for performing additional speed alteration of said data.

18. The core in claim 17, wherein said buffers comprise elastic first-in, first-out (FIFO) buffers.

19. The core in claim 15, wherein said selector comprises a multiplexor.

20. The core in claim 15, wherein additional speed adjustment is attained by said selector engaging additional lanes.

21. The core in claim 15, wherein said transmission media operates at a different data speed than said processor.